Listing of Claims

1. (Currently amended) A parallel processor comprising:

a plurality of [non-volatile memory cells] shared memory cells, each shared memory cell comprising a single non-volatile memory cell integrated with a single DRAM cell;

a plurality of processor elements, each processor element being integrated with a [non-volatile] shared memory cell, each processor elements accessing data from a corresponding [non-volatile] shared memory cell that is [most proximate to] integrated with the processor element, and performing processing on the data.

2. (Original) The parallel processor of claim 1, wherein the non-volatile memory cells comprise magnetic memory cells.

3. (Original) The parallel processor of claim 1, wherein each processor element can access a plurality of non-volatile memory cells.

4. (Currently amended) The parallel processor of claim 2, wherein each [non-volatile memory cell] magnetic memory cell is interfaced with a corresponding [at least] one dynamic random access memory (DRAM) cell.

5. (Cancel) The parallel processor of claim 2, wherein each magnetic memory cell is formed adjacent to a substrate, and the corresponding processor element is formed in the substrate proximate and adjacent to the magnetic memory cell.

6. (Cancel) The parallel processor of claim 1, wherein each magnetic memory cell is formed adjacent to a substrate, and the corresponding processor element and DRAM cell are formed in the substrate proximate and adjacent to the magnetic memory cell.

7. (Original) The parallel processor of claim 1, further comprising:

a master processor for receiving processed data from the plurality of processor elements.

8. (Original) The parallel processor of claim 7, wherein the master processor performs additional processing of the data.

9. (Original) The parallel processor of claim 1, further comprising:
an array of image sensors, an image sensor corresponding with each of the magnetic memory cells.

10. (Previously presented) The parallel processor of claim 9, wherein each image sensor receives image data that can be stored in the corresponding non-volatile memory element.

11. (Original) The parallel processor of claim 10, wherein each processing element performs processing on the image data stored in a corresponding non-volatile memory element.

12. (Currently amended) The parallel processor of claim 10, wherein the received image data is additionally stored in at least one DRAM cell [corresponding] integrated with the non-volatile memory element.

13. (Original) The parallel processor of claim 9, wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element.

14. (Original) The parallel processor of claim 12, wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate

comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element.

15. (Currently amended) The parallel processor of claim 1, further comprising:

an array of display pixels, [a] each display pixel [corresponding] integrated with a non-volatile memory cell.

16. (Currently amended) The parallel processor of claim 15, wherein each display pixel displays image data that is stored in the [corresponding] integrated non-volatile memory element.

17. (Currently amended) The parallel processor of claim 15, wherein each processing element performs processing on the image data stored in [a corresponding] the integrated non-volatile memory element.

18. (Currently amended) The parallel processor of claim 15, wherein the received image data is additionally stored in [at least] one DRAM cell [corresponding] integrated with the non-volatile memory element.

19. (Currently amended) The parallel processor of claim 15, wherein [at least one] a display pixel receives image data from a [plurality of] a non-volatile memory element[s], and wherein the display pixel is an LED and a bias current of the LED is dependent upon a resistance of the non-volatile memory element.

20. (Cancel) The parallel processor of claim 15, wherein each display pixel is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element.

21. (Original) The parallel processor of claim 18, wherein each display pixel is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element.

22. (Currently amended) A method of parallel processing, comprising:

storing data in a plurality of non-volatile memory cells;

processing the data with a plurality of processor elements which are integrated with the non-volatile memory cells and DRAM cells,]each non-volatile memory cell corresponding with a most proximate processor element,] each processor element accessing data from the [corresponding] integrated non-volatile memory cell and integrated DRAM cell, and performing processing on the data.

23. (Currently amended) A computing system comprising:

a central processing unit;

a parallel processor connected to the central processing unit, the parallel processor comprising:

a plurality of processor elements, each processor element being integrated with a non-volatile memory cell, each processor elements accessing data from the non-volatile memory cell and an integrated DRAM cell, and that [is] are most proximate to the processor element, and performing processing on the data.

24. (Currently amended) The parallel processor of claim 4, wherein a word line (WL) is connected to [each non-volatile] a magnetic memory cell and a corresponding dynamic random access memory (DRAM) cell.

25. (Currently amended) The parallel processor of claim 24, the word line (WL) is connected a MRAM controlling transistor of the non-volatile memory and to a DRAM controlling transistor of the dynamic random access memory (DRAM)

cell, and wherein a first metallization layer forms conductive contacts to an MRAM gate of the MRAM controlling transistor, a DRAM gate of the DRAM controlling transistor and to a DRAM capacitor, a second metallization layer forms a conductive contact to the non-volatile memory, a third metallization layer forms another conductive contact to the non-volatile memory, and a fourth metallization layer forms a non-volatile memory write word line.

26. (Cancel) The parallel processor of claim 5, wherein the corresponding processor element is formed in the substrate most proximate to the magnetic memory cell.

27. (Cancel) The parallel processor of claim 6, wherein the corresponding processor element and DRAM cell are formed in the substrate most proximate to the magnetic memory cell.

28. (Previously presented) The parallel processor of claim 9, wherein the image sensor corresponding with a magnetic memory cell is the image sensor most proximate to the magnetic memory cell.

29. (Cancel) The parallel processor of claim 15, wherein the display pixel corresponding with a non-volatile memory cell is the display pixel most proximate to that is integrated with the non-volatile memory cell.